CLAIMS

1. A wireless communication architecture, comprising:

a virtual channel memory controller;

first and second processor cores coupled to the virtual channel memory controller;

a first synchronous memory device coupled to the virtual channel memory controller by a dedicated first data bus;

a second synchronous memory device coupled to the virtual channel memory controller by a dedicated second data bus;

a shared address and control bus interconnecting the virtual channel memory controller and the first and second synchronous memory devices.

2. The architecture of Claim 1, the virtual channel memory controller having address bus arbitration logic coupled to the first and second memory controllers, and a multiplexer interconnecting the first and second memory controllers to the shared address and control bus.

3. The architecture of Claim 1, the first synchronous memory device is SRAM/SDRAM memory, the second synchronous memory device is burst Flash/ROM memory.

4. The architecture of Claim 1, the virtual channel memory controller having a group of shared memory space access registers interconnecting first and second processor core memory access register blocks, the first processor core memory access block coupled to the first processor core, the second processor core memory access block coupled to the second processor core.

5. The architecture of Claim 1, a first direct memory access channel coupled to the virtual channel memory controller, a second direct memory access channel coupled to the virtual channel memory controller.

6. The Architecture of Claim 1, a display controller coupled to the virtual channel memory controller, the direct memory access channel and the display controller are disposed on the integrated circuit.

7. The architecture of Claim 1, the first processor core is a digital signal processor, the second processor core is a RISC processor.

8. The architecture of Claim 1, the virtual channel memory controller and the first and second processor cores are disposed on a single integrated circuit.

9. A virtual channel shared memory architecture, comprising:

a virtual channel memory controller;

a first synchronous memory device coupled to the virtual channel memory controller by a first data bus;

a second synchronous memory device coupled to the virtual channel memory controller by a second data bus;

a shared address and control bus interconnecting the virtual channel memory controller and the first and second synchronous memory devices.

10. The architecture of Claim 9, the virtual channel memory controller having address bus arbitration logic coupled to the first and second memory controllers, a multiplexer interconnecting the first and second memory controllers to the shared address and control bus.

11. The architecture of Claim 9, the first synchronous memory device is SRAM/SDRAM memory, the second synchronous memory device is burst Flash/ROM memory.

12. The architecture of Claim 9, the virtual channel memory controller having a group of shared memory space access registers interconnecting first and second processor core memory access register blocks, the first processor core memory access block coupled to the first processor core, the second processor core memory access block coupled to the second processor core.

13. A method in a virtual channel shared memory system architecture, comprising:

addressing first and second synchronous memory devices with a shared address bus interconnecting the first and second synchronous memory devices and a virtual channel memory controller;

accessing the first synchronous memory device via a first data bus interconnecting the first synchronous memory device and the virtual channel memory controller;

accessing the second synchronous memory device via a second data bus interconnecting the second synchronous memory device and the virtual channel memory controller.

14. The method of Claim 13, concurrently accessing the first and second synchronous memory devices.

15. The method of Claim 13, addressing the first synchronous memory device, accessing the first synchronous memory device in response to addressing the first synchronous memory device, addressing the second synchronous memory device after addressing the first synchronous memory device, accessing the second synchronous memory device in response to addressing the second synchronous memory device while accessing the first synchronous memory device.

16. The method of Claim 13, addressing one of the first and second synchronous memory devices while accessing the first and second synchronous memory devices.

17. The method of Claim 13, reducing power consumption by maintaining a state of the shared address bus during an interval between addressing the first and second synchronous memory devices.

18. The method of Claim 13, resolving requests from first and second memory controllers for use of the shared address bus with address bus arbitration logic, routing address signals from the first and second memory controllers to the shared address bus with a multiplexer.

19. The method of Claim 13, conveying access permission to shared memory space with a group of registers indicating shared memory space policy, facilitating communication between first and second processor cores with shared memory space by passing data by reference.

20. The method of Claim 13, reducing latency by addressing one of the first and second synchronous memory devices while accessing the same memory device addressed.

21. A method in a wireless communication architecture, comprising:

addressing first and second synchronous memory devices with a shared address bus interconnecting the first and second synchronous memory devices and a virtual channel memory controller;

transferring data between the first synchronous memory device and the virtual channel memory controller on a first data bus;

transferring data between the second synchronous memory device and the virtual channel memory controller on a second data bus.

22. The method of Claim 21, concurrently accessing the first and second synchronous memory devices.

23. The method of Claim 21, addressing the first synchronous memory device with the shared address bus, transferring data between the first synchronous memory device and the virtual channel memory controller in response to addressing the first synchronous memory device, addressing the second synchronous memory device with the shared address bus after addressing the first synchronous memory device, transferring data between the second synchronous memory device and the virtual channel memory controller in response to addressing the second synchronous memory device while transferring data between the first synchronous memory device and the virtual channel memory controller.

24. The method of Claim 21, reducing latency by addressing one of the first and second synchronous memory devices while accessing the same memory device addressed.

25. The method of Claim 21, reducing power consumption by not changing a state of the shared address bus during an interval between addressing the first and second synchronous memory devices.